

WHAT IS CLAIMED IS:

1. A phase-change memory device comprising:
memory cells including phase-change layers formed
on a semiconductor substrate, the phase-change layer
5 showing an amorphous-crystalline phase change;

a memory cell array which has the memory cells
arranged in a matrix, the phase change layer including
first regions which contact the semiconductor substrate
in units of memory cells and a second region which
10 connects the first regions arranged in a same column;

a first electrode layer formed on the second
region of each phase-change layer, a contact area of
each first region and the semiconductor substrate being
smaller than a contact area of the second region and
15 the first electrode layer;

a word line which connects the memory cells
arranged in a same row; and

a bit line electrically connected to the first
electrode layer, the bit line connecting in common the
20 phase-change layers of the memory cells arranged in the
same column.

2. The device according to claim 1, further
comprising a contact plug which connects the first
electrode layer and the bit line.

25 3. The device according to claim 1, wherein each
phase-change layer further includes a third region
interposed between the second region and each first

region, the third region having a width greater than the contact area of each first region and the semiconductor substrate, and less than the contact area of the second region and the first electrode layer.

5 4. The device according to claim 1, further comprising a resistor element formed on the semiconductor substrate with respect to each memory cell and provided for each memory cell between the semiconductor substrate and the first region of each
10 phase-change layer, a contact area of the resistor element and each first region being smaller than the contact area of the second region and the first electrode layer.

 5. The device according to claim 1, further
15 comprising a second electrode layer interposed between each first region and the semiconductor substrate.

 6. The device according to claim 5, wherein an upper surface of the second electrode layer opposing each first region is larger than a surface of each
20 first region opposing the second electrode layer.

 7. The device according to claim 1, wherein each memory cell further includes a bipolar transistor formed in the semiconductor substrate, a collector or an emitter of the bipolar transistor being connected to
25 a corresponding one of the first regions, a base of the bipolar transistor being connected to the word line.

 8. The device according to claim 1, wherein each

memory cell further includes a MOS transistor formed on the semiconductor substrate, a source or a drain of the MOS transistor being connected to a corresponding one of the first regions, a gate of the bipolar transistor being connected to the word line.

9. The device according to claim 1, wherein the second region of each phase-change layer is in a crystalline state, and at least part of each first region of each phase-change layer assumes one of the crystalline state and an amorphous state in accordance with write data.

10. A phase-change memory device comprising:
memory cells including a phase-change layer formed on a semiconductor substrate, the phase-change layer showing an amorphous-crystalline phase change;

a memory cell array which has the memory cells arranged in a matrix;

a word line which connects the memory cells arranged in a same row; and

a bit line which connects the phase-change layers of the memory cells arranged in a same column, each of the phase-change layers including first regions which contact the semiconductor substrate in units of memory cells and a second region which connects the first regions arranged in the same column and which contacts the bit line, a contact area of each first region and the semiconductor substrate being smaller than

a contact area of the second region and the bit line.

11. The device according to claim 10, wherein the bit line includes a first metal layer and a second metal layer contacting the second region.

5 12. The device according to claim 11, wherein the first metal layer has a lower resistance than the second metal layer.

10 13. The device according to claim 10, wherein each phase-change layer further includes a third region interposed between the second region and each first region, the third region having a width greater than the contact area of the each first region and the semiconductor substrate, and less than the contact area of the second region and the bit line.

15 14. The device according to claim 10, further comprising a resistor element formed on the semiconductor substrate with respect to each memory cell and provided between the semiconductor substrate and the first region of each phase-change layer, a
20 contact area of the resistor element and each first region being smaller than the contact area of the second region and the bit line.

25 15. The device according to claim 10, further comprising a second electrode layer interposed between each first region and the semiconductor substrate.

16. The device according to claim 15, wherein an upper surface of the second electrode layer opposing

each first region is larger than a surface of each first region opposing the second electrode layer.

17. The device according to claim 10, wherein each memory cell further includes a bipolar transistor
5 formed in the semiconductor substrate, a collector or an emitter of the bipolar transistor being connected to a corresponding one of the first regions, a base of the bipolar transistor being connected to the word line.

18. The device according to claim 10, wherein each
10 memory cell further includes a MOS transistor formed on the semiconductor substrate, a source or a drain of the MOS transistor being connected to a corresponding one of the first regions, a gate of the bipolar transistor being connected to the word line.

15 19. The device according to claim 10, wherein the second region of each phase-change layer is in a crystalline state, and at least part of each first region of each phase-change layer assumes one of the crystalline state and an amorphous state in accordance
20 with write data.